REMARKS/ARGUMENTS

Favorable reconsideration of this application is requested.

Claims 1, 2, 4, 6, 10, 16-19 and 21-30 are present in this application, claims 5, 7, 8, 11-15 and 20 being canceled and claims 22-30 being added by way of the present amendment. Amended claim 1 is supported by, for example, the non-limiting disclosure on page 79, line 24 to page 80, line 10 of the specification, Figure 150 and page 323, lines 16 to 23. Amended claim 2 is supported by, for example, the non-limiting disclosure in Fig. 1. New claim 22 is supported by, for example, the non-limiting disclosure on page 227, line 18 to page 228, line 2; page 229, lines 5-11; page 250, lines 1-11; page 304, lines 21-25; and page 305, lines 1-20; and Figures 54 and 55.

Non-limiting examples of the support for new claims 23-30 is also provided in the table below:

Claim 23	Figure 42 and line 17, page 264 to line 6, page 265
Claim 24	Figures 54 and 55; page 229, lines 5-11, page 305, lines 9-20; page 306, lines 13-17, page 306
Claim 25	Figures 75 and 76; page 273, line 12 to page 275, line 15
Claim 26	Figures 43, 54, 55 and 150; page 70, line 24 to page 80, line 5; page 266, lines 4-6; page 304, lines 21-25
Claim 27	Page 221, lines 20-24 and page 395, line 21 to page 396, line 2
Claim 28	Page 128, lines 20-22
Claim 29	Page 79, line 24 to page 80, line 5
Claim 30	Page 50, lines 3-4

Accordingly, no question of introduction of new matter is believed to be raised by the amended claims.

Claims 1 and 2 recite:

EL elements arranged in a matrix;

driver transistors which supply current to be passed through the EL elements;

a first condenser having a first terminal and a second terminal;

first switching elements placed in current paths of the EL elements;

a switching transistor which is connected between a gate terminal and the other terminal of said driver transistor; and

a gate driver circuit which turns on and off the first switching elements for control;

wherein:

said first terminal of the first condenser is connected to said gate terminal of the driver transistor,

said second terminal of the first condenser is connected to an electrode to which predetermined voltage is impressed, and

said switching transistor has a multi-gate structure.

The device with switching transistor with a multi-gate structure improves the off-leakage characteristic, that is, it does not generate the off-leakage current. Further, excellent stripe image displays can be generated (please see, as a non-limiting example, Figures 16(b) and 19(b1)-(c3)).

Claims 1 and 2 additionally recite a plurality of stripe non-display areas on said display screen of the EL display panel are generated and the plurality of stripe non-display areas are moved in scanning direction of the gate driver circuit at a cycle of one frame period Since the frame rate of image display can be lowered, it is possible to reduce the power consumption and to reduce the generating of the flicker as an advantageous effect. As further advantageous effect, since the proportion of the plurality of stripe non-display areas in the entire display screen can be changed, it is possible to control the display brightness of the screen.

Claims 1, 2, 4-7, 10 and 15-21 are rejected under 35 U.S.C. §103(a) over US 6,583,775 (Sekiya et al.) in view of U.S. 2002/0126107 (Inoue et al.).

In the drive method of claims 1 and 2, the second terminal of a first condenser is connected to an electrode to which a predetermined voltage is impressed, and one terminal of a first switching element is connected with the EL element. In contrast, Figure 5 of Sekiya et al. shows that the both of the terminal of condenser Cs and source terminal S of TFT3 are connected with the common potential (GND). The pixel shown in Figure 5 of Sekiya et al. is different from the structure of the panel in the drive method of claims 1 and 2. Further, a switching transistor having a multi-gate structure is neither disclosed nor suggested by Sekiya et al. Sekiya et al. cannot provide the advantageous effects of avoiding off-leakage current and achieving a high-quality display.

Inoue et al. is asserted to teach generating a plurality of stripe non-display areas on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit. However, the Applicants respectfully traverse this assertion. In Inoue et al., a drive method is disclosed which generates a non-display region (for example, a pixel region scanned by the first to 40th scanning lines from the top of the liquid crystal panel 100, and a pixel region scanned by 61th to 200th scanning lines as shown in Figure 6) and a display region (a pixel region scanned by 41th to 60th scanning lines as shown in Figure 6) on the liquid crystal panel. However, Inoue et al. discloses that "[n]ext, the scanning signal in the case of performing a partial display operation is studied hereinbelow. It is assumed herein that the partial display as shown in FIG. 6 is realized, practically, and a pixel region scanned by the first to 40th scanning lines from the top of the liquid crystal panel 100, as viewed in this figure, and a pixel region scanned by 61th to 200th scanning lines are non-display regions, while a pixel region scanned by 41th to 60th scanning lines is a display region" (emphasis added, please see [0075]; see also Figure 6 and the description three lines from the bottom of paragraph [0004] of Inoue et al.).

It is clear that the non-display regions and display region of Inoue (for example, see Figures 6 and 12) are fixed on the liquid crystal panel 100 and are not moved in the scanning direction of the gate driver circuit at a cycle of one frame period as recited in claims 1 and 2. Further, Inoue et al. does not disclose the structure of EL element nor a switching transistor having a multi-gate structure as recited in claims 1 and 2.

It is respectfully submitted that Sekiya et al. and Inoue et al. neither disclose nor suggest the drive methods of claims 1 and 2. Claims 1 and 2 are patentably distinguishable over the combination of these two references.

Claims 4, 6, 10, 16-19 and 21 depend from claims 1 and 2 and are patentable over the above cited references for the same reasons discussed above for claims 1 and 2.

New claim 22 recites "said non-display area is moved in a scanning direction of said gate driver circuit at a cycle of frame period," which is not suggested by Sekiya et al. and Inoue et al., as discussed above. Claim 22 also recites "said gate driver circuit turns on said third switching element to impress a first voltage to a selected line of the pixels," "said image signal is impressed to said line of the pixels after said first voltage is impressed to said line of the pixels" and "said non-display area is moved in a scanning direction of said gate driver circuit at a cycle of frame period," which are not believed to be disclosed by the cited prior art.

It is respectfully submitted that the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

Respectfully submitted,

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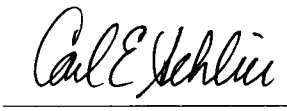

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